

What is claimed is:

- 1 1. A method for forming a semiconductor device comprising:
2 providing a structure of a semiconductive material with a hardmask thereover,
3 said hardmask having at least one tapered portion with a corresponding portion of a
4 further film disposed thereover;
5 etching an uncovered portion of said hardmask to expose an exposed portion of
6 said semiconductive material while maintaining said at least one tapered portion and
7 each said corresponding portion substantially intact; and
8 etching said exposed portion of said semiconductive material while maintaining
9 said at least one tapered portion and each said corresponding portion substantially
10 intact.
- 1 2. The method as in claim 1, wherein said providing comprises providing said
2 hardmask with an originally tapered upper surface covered by said further film, and
3 removing a first portion of said originally tapered upper surface and a first portion of said
4 further film to produce said hardmask having said at least one tapered portion with a
5 corresponding portion of said further film disposed thereover, and said uncovered
6 portion.
- 1 3. The method as in claim 2, wherein said removing comprises chemical
2 mechanical polishing.
- 1 4. The method as in claim 2, wherein said further film comprises an oxide
2 liner and said removing includes forming a spacer oxide material over said further film
3 and etching portions of said spacer oxide material and said first portion of said further
4 film.
- 1 5. The method as in claim 4, wherein said removing further includes, after
2 said etching said portions of spacer oxide material and said first portion, forming an etch
3 stop layer thereover and an interlevel dielectric over said etch stop layer, then
4 planarizing such that said uncovered portion of said hardmask is planarized.

1 6. The method as in claim 1, wherein said further film comprises an oxide
2 film.

1 7. The method as in claim 6, wherein said etching an uncovered portion of
2 said hardmask includes a hardmask:further film etch selectivity ranging from 5:1 to 10:1.

1 8. The method as in claim 1, wherein said semiconductive material
2 comprises polycrystalline silicon.

1 9. The method as in claim 1, wherein, after said etching said exposed portion
2 of said semiconductive material, removing said at least one tapered portion with a
3 corresponding portion of a further film disposed thereover, thereby producing at least
4 one corresponding gate structure of said semiconductive material.

1 10. The method as in claim 9, wherein each of said at least one corresponding
2 gate structure includes a width of about 10 nanometers.

1 11. The method as in claim 1, wherein said structure of a semiconductive
2 material includes a width within the range of 50 to 500 nanometers.

1 12. The method as in claim 1, wherein said etching said subjacent portion of
2 said semiconductive material includes a semiconductive material:hardmask etch
3 selectivity ranging from 50:1 to 100:1.

1 13. The method as in claim 1, wherein said hardmask is formed of SiN or
2 SiON.

1 14. The method as claim 1, wherein said providing includes providing a layer
2 of material of said hardmask over a semiconductor substrate surface and etching to
3 produce said hardmask having at least one tapered portion, each tapered portion
4 having a taper angle within the range of 45° to 85° with respect to said semiconductor
5 substrate surface.

1 15. A method for forming a semiconductor device comprising:
2 providing a layer of hardmask material over a semiconductor substrate;

3 forming a photoresist pattern over said layer of hardmask material;
4 etching to produce a discrete portion of said hardmask material, said discrete
5 portion having at least one tapered section with a taper angle within the range of 45° to
6 85° with respect to a surface of said semiconductor substrate;
7 carrying out a photoresist strip process;
8 forming an oxide layer over said discrete portion;
9 removing portions of said oxide layer and planarizing to produce said discrete
10 portion having a substantially planar uncovered portion and each tapered section having
11 a corresponding portion of said oxide layer thereover.

1 16. The method as in claim 15, in which said etching includes at least one
2 etchant species chosen from the group consisting of CF₄, CHF₃, CH₂F₂, CH₃F, C₅F₈,
3 CO, Ar, and O₂.

1 17. A semiconductor device comprising a semiconductive material formed
2 over a substrate, having a width no greater than 10 nm and a top surface substantially
3 parallel to said substrate, a hardmask formed on said top surface and having an angled
4 upper surface and an oxide film formed thereover, said angled upper surface and said
5 top surface forming an angle ranging from 45° to 85°.

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2 18. The semiconductor device as in claim 17, wherein said semiconductive
3 material comprises polysilicon.

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2 19. The semiconductor device as in claim 18, wherein said hardmask is
3 formed of SiN or SiON.

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2 20. A semiconductor device comprising a discrete semiconductive material
3 structure formed over a substrate surface and having a top surface substantially parallel
4 to said substrate surface, said structure including at least one masked portion having a
5 hardmask formed on said top surface, said hardmask having an angled upper surface

6 and an oxide film formed thereover, said angled upper surface and said top surface
7 forming an angle ranging from 45° to 85°.

1 21. The semiconductor device as in claim 1, wherein said hardmask is formed
2 of SiN or SiON.

1 22. The semiconductor device as in claim 1, wherein said at least one masked
2 portion comprises a duality of said masked portions disposed at opposed ends of said
3 discrete semiconductive material structure.